GALAXYCORE INC.

VGA CMOS IMAGE SENSOR

GC0303V1

Version1.3

Contents

General Description

GC0303V1 is a digital CMOS Image Sensor, which can be used for Camera Phone, PC Camera that requires VGA (640x480) resolution. The chip is programmable through a simple two-wire serial interface. Pixel data is output via an 8/10-bit raw RGB data bus, along with a pixel clock, which is synchronous with the valid data.

The sensor can be operated in its default mode or programmed by the user for frame rate, exposure time, black level composition, gain setting and other parameters. An on chip analog-to-digital converter (ADC) provides a 10-bit data per pixel.

Table 1 Technical Parameters

Parameters	Values
Optical format	1/4” (diagonal)
Pixels Array size	640 x 480 (without border)
	654 x 490 (with border)
Pixel size	5.15um x 5.15um
Frame rate	0.5 ~ 30 fps, continuous
Scan format	Progressive
Electronic programmable shutter	0 rows to 4095 rows
Optical Fill factor	~ 50% (w/o microlens)
Pixel-to-pixel FPN	0.3% p-p of sat
Column-to-column FPN	0.3% p-p of sat
Peak SNR	>45 dB
A/D Converter	10-bit
Color pattern	Primary Bayer checkerboard
Power supply voltage	1.8V/ 2.8V
Power supply current (operating)	25 mA
Power supply current (standby)	<10 uA @2.8V
Operation temperature	-20~60° C
Storage temperature	-40~85° C
Packaging	28-pin PLCC / Wafer

Figure 1 Sensor Interface

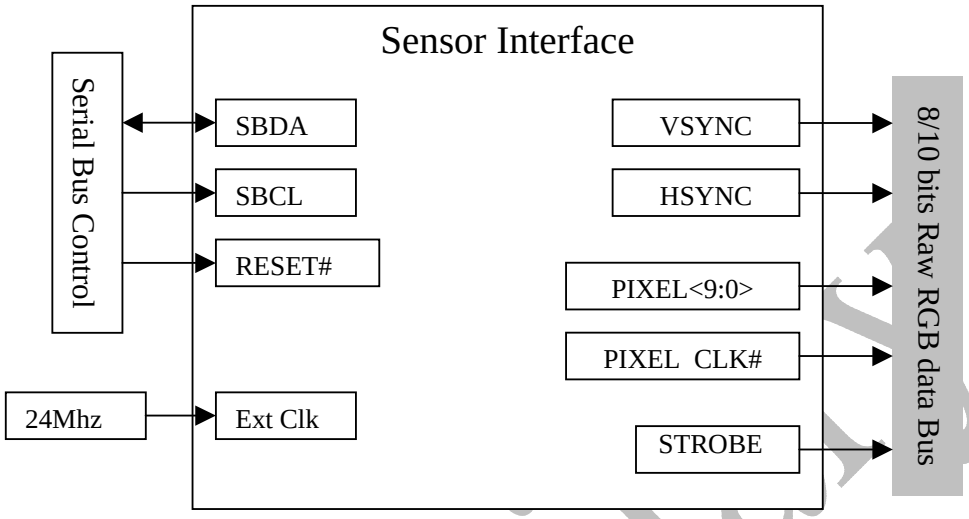
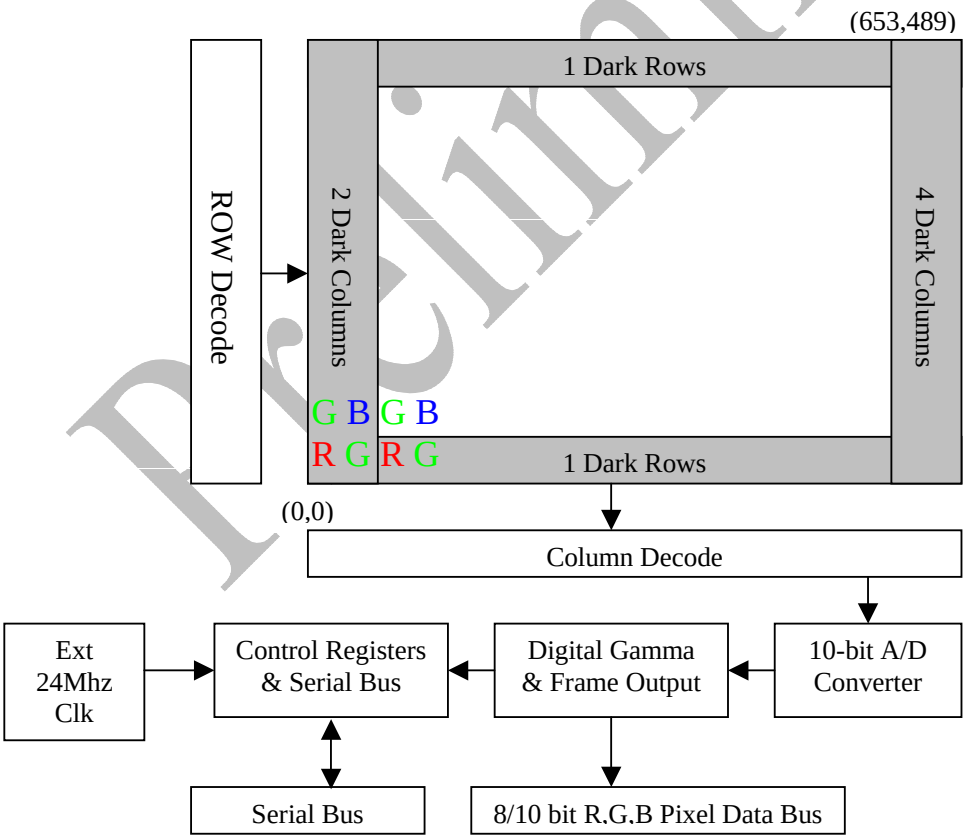


Figure 2 Block Diagram



Serial Communication Interface

1. Protocol

Device Address: serial bus read address = 31H, serial bus write address = 30H.

The host must perform the role of a communications master and GC0303V1 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.

Figure 3 Serial Communication State Diagram

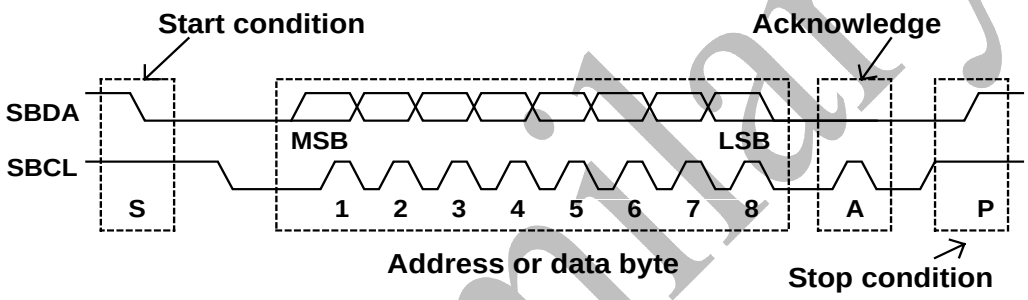


Figure 4 Registers Incremental Writing

S	30H	A	Address	A	Data1	…	A	DataN	A	P

Note ----- S: Start P: Stop A: Acknowledge
30H: Writing Address (8 bits)
31H: Reading Address (8 bits)
Address: Register Address (8 bits)
Data, Data1, DataN: Writing data (8 bits)

2. Serial Bus Timing

Figure 4 Serial Bus Timing Diagram

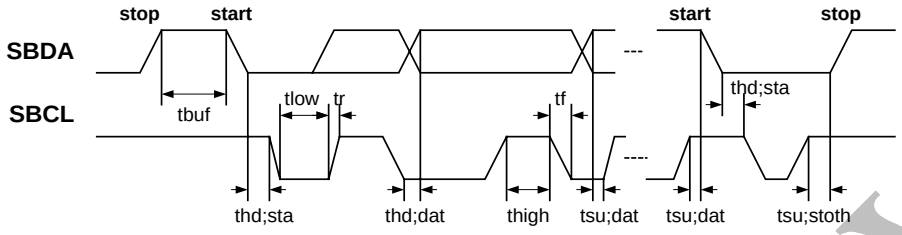


Table 2 Parameters

Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a **stop** and a **start**	tbuf	1.2	*	μs
Hold time for a repeated **start**	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated **start**	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

DC Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
VDD-A	DC supply voltage – Analog		2.6	2.8	2.9	V
VDD-C	DC supply voltage – Core		1.6	1.8	2.0	V
VDD-D	DC supply voltage – Digital		2.5	2.8	3.1	V
Vih	Input voltage logic "1"		2.0	2.8		V
Vil	Input voltage logic "0"		-	0	0.6	V
Voh	Onput voltage logic "1"		2.5	2.8		V
Vol	Onput voltage logic "0"		-	0	0.3	V
I_{DD}	operating Current	25fps@24MHz	-	-	20	mA
I_{DD} standby	Standby Supply Current		-	-	10	uA

AC Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
fclk_in	Input Clock Frequency			24		MHz
t_{CLK}	Input Clock Period			42		ns
$t_{CLK:DC}$	Clock Duty Cycle		45	50	55	%
t_{SU}	PCLK to DOUT<9:0> Setup Time			15		ns
t_{HD}	PCLK to DOUT<9:0> hold Time			15		ns
t_{PHH}	PCLK[↓] to HSYNC[↑]			12		ns
t_{PHL}	PCLK[↓] to HSYNC[↓]			12		ns

Pixel Data Format

1. Clock

Main clock will be generated by input external 24MHZ clock and register Npl. (refer to Table 3 register definition). So, the Main clock rate can be 1, 1/2, 1/4, 1/8 input external clock rate by setting register Npl. Then generate analog clock and digital clock. Normally, 8/10 bits RGB data will be read out by PIXEL_CLK.

2. Pixel Color Pattern

GC0303 uses the RGB Bayer color pattern. Even numbered rows contain green and red color pixels, and odd numbered rows contain blue and green color pixels. Likewise, even numbered columns contain green and blue color pixels, and odd numbered columns contain red and green color pixels.

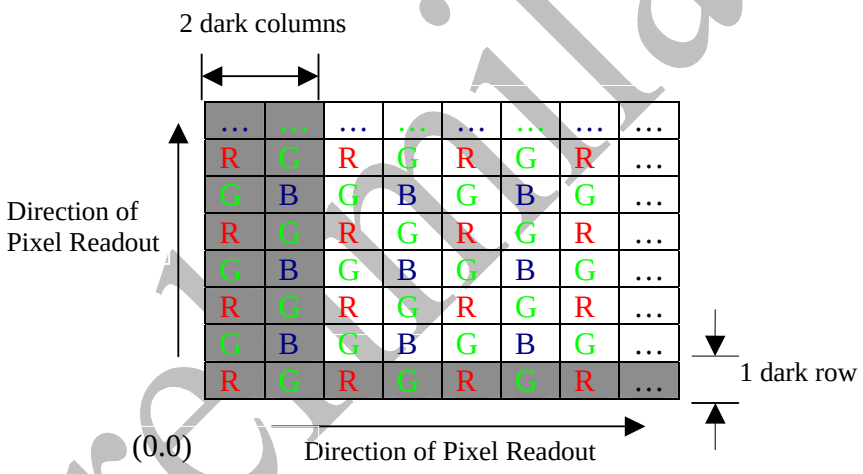


Figure 5. RGB Bayer Color Pattern Details (Bottom Left Corner)

3. Output Frame Format

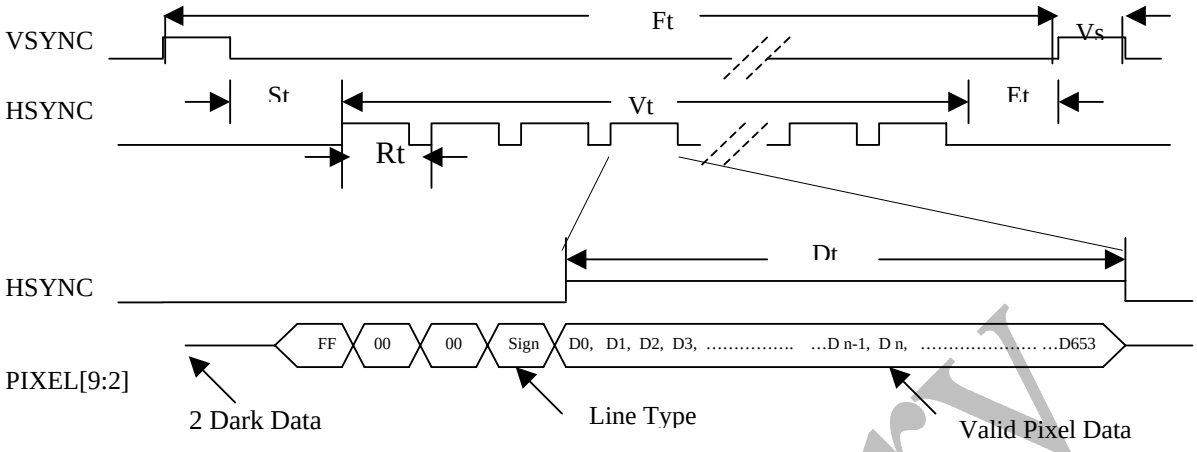


Figure 6 Frame Format Timing

There are two modes for video output interface: one with vertical frame sync and horizontal line sync indicated by output pin VSYNC and HSYNC, another with the sync information embedded in data bus PIXEL[9:2]. For both modes, the line formats are the same; the pixel data formats are also the same.

When start a new frame, VSYNC rise to high, after one row time period, it become to low. And after Frame Start time, HSYNC rise to high to indicate a pixel data line start and valid Pixel data will be outputted for both mode. But for the mode supported the embedded "Line type", a new line start mark 0xFF, 0x00, 0x00, will be output first, and follow line type byte, Before the valid pixel data bus output. The type is defined as

Line Type Byte	Line Type
F1	Dark Line
DA	Pixel Line

Table 3. Frame Time with default setting:

Parameter	Name	EQUATION
Dt	Valid pixel data time	Valid Pixel Data length, Max = 654;
Rt	Row time	Rt = 844 + Hb; Hb is defined by Reg0x01 （default =72）
Vt	Active Data Time	Vt = Rt*(256*Reg0x96+Reg0x97); (default =482）
St	Frame Start time	St = 4*Rt ;
Vb	Vertical Blanking	Vb is defined by Reg0x02 (default =34)
Et	Frame End time	Et = (489+Vb-Vt-St)* Rt; = 4*Rt
Vs	VSYNC High Time	Vs = Reg0xa0[bit5,6,7]* Rt; (default=1)
Ft	Total Frame time	Ft = Vs + St + Vt + Et = (490+ Vb) * (844 + Hb); = 524 * 916 (for 24Mhz clk 25 f/second)

Table 4 Register Definition:

Chip Version – Address: 80H Default: 11H

Bit	Name	Read/Write	Description
3-0	Version	Read Only	Version Number : 0x1
7-4	Type	Read Only	Product Type : VGA 0x1

Horizontal Blank Line Register – Address 0x81h Default: 48H

Bit	Name	Read/Write	Description
6-0	Hb<6:0>	R/W	HSYNC blanking time Total blank = 184 + Hb cols. Default 0x48H (d72)
7-6	Reserved		

Vertical Blank Line Register – Address 0x82h Default: 22H

Bit	Name	Read/Write	Description
7-0	Vb<7:0>	R/W	Frame Rate Control 1 Row to 255 Rows. If Expose time < Vb + 490, Frame Rate will controlled by Vb + 490. Else, Frame Rate will be controlled by Exp Register Value. Default 0x22H (34 Rows)

Expose High Register – Address 0x83h Default: 1H

Bit	Name	Read/Write	Description
3-0	ExpH<3:0>	R/W	Expose High Register Expose time = ExpH*256+ExpL (262 rows) Default 0x1H

Expose Low Register – Address 0x84h Default: 06H

Bit	Name	Read/Write	Description
7-0	ExpL<7:0>	R/W	Expose Low Register Default 0x06 H

Global Background Composition – Address 0x85h Default: 00H

Bit	Name	Read/Write	Description
7-0	BgComp	R/W	Background Dark Level (-32 ~ 31) Data is 2's Complementary Code. -128 ~ +127 Default 0x0

GRED Background Composition – Address 0x86h Default: 00H

Bit	Name	Read/Write	Description
4-0	Red_level	R/W	Red Background Dark Level Data is 2's Complementary Code. Range: -16 ~ +15 Default 0x0
7-5	Reserved		

RED Background Composition – Address 0x87h Default: 00H

Bit	Name	Read/Write	Description
4-0	Gred_level	R/W	Green Background Dark Level (in red line) Data is 2's Complementary Code. Range: -16 ~ +15 Default 0x0
7-5	Reserved		

GBLUE Background Composition – Address 0x88h Default: 00H

Bit	Name	Read/Write	Description
4-0	Blue_level	R/W	Blue Background Dark Level Data is 2's Complementary Code. Range: -16 ~ +15 Default 0x0
7-5	Reserved		

BLUE Background Composition – Address 0x89h Default: 00H

Bit	Name	Read/Write	Description
4-0	Gblue_level	R/W	Green Background Dark Level (in blue line) Data is 2's Complementary Code. Range: -16 ~ +15 Default 0x0
7-5	Reserved		

GRED Gain Control High Register – Address 0x8ah Default: 01H

Bit	Name	Read/Write	Description
2-0	RedgH	R/W	Red Pixel Gain High Byte Gain Value = RedgL/256 + RedgH; Range: 0 to 7 Default 0x01
7-3	Reserved		

GRED Gain Control Low Register – Address 0x8bh Default: 30H

Bit	Name	Read/Write	Description
7-0	RedgL	R/W	Red Pixel Gain Low Byte Range: 0 to 255 Default 0x30

RED Gain Control High Register – Address 0x8ch Default: 01H

Bit	Name	Read/Write	Description
2-0	GredgH	R/W	Green Pixel Gain High Byte (in red line) Gain Value = GredgL/256 + GredgH; Range: 0 to 7 Default 0x01
7-3	Reserved		

RED Gain Control Low Register – Address 0x8dh Default: 30H

Bit	Name	Read/Write	Description
7-0	GredgL	R/W	Green Pixel Gain Low Byte (in red line) Range: 0 to 255 Default 0x30

BG Gain Control High Register – Address 0x8eh Default: 01H

Bit	Name	Read/Write	Description
2-0	GbgH	R/W	Green Pixel Gain High Byte (in blue line) Gain Value = GbgL / 256 + GbgH; Range: 0 to 7 Default 0x01
7-3	Reserved		

BG Gain Control Low Register – Address 0x8fh Default: 30H

Bit	Name	Read/Write	Description
7-0	GbgL	R/W	Green Pixel Gain Low Byte (in blue line) Range: 0 to 255 Default 0x30

GBG Gain Control High Register – Address 0x90h Default: 01H

Bit	Name	Read/Write	Description
2-0	BgH	R/W	Blue Pixel Gain High Byte Gain Value = BgL/ 256 + BgH, Range: 0 to 7 Default 0x01
7-3	Reserved		

GBG Gain Control Low Register – Address 0x91h Default: 30H

Bit	Name	Read/Write	Description
7-0	BgL	R/W	Blue Pixel Gain Low Byte Range: 0 to 255 Default 0x30H

Row Start Control High Register – Address: 92H Default: 00H

Bit	Name	Read/Write	Description
0	RowH	R/W	Row Starting High Byte RowH+RowL Range : 0 ~ (489 – Win height) Default 0x0
7-6	Reserved		

Row Start Control Low Register – Address: 93H Default: 04H

Bit	Name	Read/Write	Description
7-0	RowL	R/W	Row Starting Low Byte Default 0x4

Col Start Control High Register – Address: 94H Default: 00H

Bit	Name	Read/Write	Description
1-0	ColH	R/W	Col Starting High Byte ColH+ColL Range: 0 ~ (648-Win width) Default 0x0
7-5	Reserved		

Col Start Control Low Register – Address: 95H Default: 06H

Bit	Name	Read/Write	Description
7-0	ColL	R/W	Col Starting Low Byte Default 0x6

Window Height Control High Register – Address: 96H Default: 01H

Bit	Name	Read/Write	Description
0	WinHH	R/W	Window Height Value High Byte WinHH+WinHL Range: 4 ~ 488 (default is 482 rows) Default 0x01
7-6	Reserved		

Window Height Control Low Register – Address: 97H Default: E2H

Bit	Name	Read/Write	Description
7-0	WinHL	R/W	Window Height Value Low Byte Default 0xE2

Window Width Control High Register – Address: 98H Default: 02H

Bit	Name	Read/Write	Description
1-0	WinWH	R/W	Window Width Value High Byte WinWH+WinWL Range: 4 ~ 648 (default: 642 Cols) Default 0x02
7-5	Reserved		

Window Width Control Low Register – Address: 99H Default: 82H

Bit	Name	Read/Write	Description
7-0	WinWL	R/W	Window Width Value Low Byte Default 0x82

Gamma Control Register – Address 0x9ah Default: 02H

Bit	Name	Read/Write	Description
3-0	Gamma	R/W	Gamma Control Gain at Zero change from 1 to 6 Range: 0 to 15 Default 0x02
7-4	Reserved		

Power Down Control Register – Address 0x9bh Default: 80H

Bit	Name	Read/Write	Description
4-0	Pdown	R/W	Power Down Control Default: 0x00
7-5	Vctrl	Read-Only	

Bias Current Control Register – Address 0x9ch Default: 15H

Bit	Name	Read/Write	Description
4-0	Bctrl	R/W	Bias Current Control bits, Default is 0x15H
7-5	Reserved		

Test Control – Address 0x9dh Default: 80H

Bit	Name	Read/Write	Description
3-0	Tcon	Read-Only	Test Control bits, default is 0x0
4	Dout	R/W	Pixel Data Output Mode 0 – Output Pixel Data 1 – Output data from ROM-CODE Default 0x0
5	Dw	R/W	Pixel Data Output Data Width 0 – 8 bit Pixel Data 1 – 10 bit Pixel Data Default 0x0
6	Strobe_ena	R/W	STROBE enable 1 – enable STROBE 0 – disable STROBE Default 0x0
7	Auto	Read-Only	Default is 0x1

Mode Control Register – Address: 9eH Default: 08H

Bit	Name	Read/Write	Description
1-0	Npl	R/W	Clock Rate Control 0 – Input Clock Rate 1 – 1/2 Input Clock Rate 2 – 1/4 Input Clock Rate 3 – 1/8 Input Clock Rate Default 0x0
7-2	SamT	R/W	Timing Control Bits, Default is 0x02

Frame Control Register – Address: 9fH Default: 00H

Bit	Name	Read/Write	Description
0	PCLKinv	R/W	Pixel Clk inversion 1 – Pixel clock inversion Default 0x0
1	HSinv	R/W	HSYNC inversion 1 – HSYNC inversion Default 0x0
2	VSinv	R/W	VSYNC inversion 0 – VSYNC high at blank rows 1 – VSYNC high at active rows Default 0x0
3	PCLKen	R/W	Block Pixel Clk at invalid data 1 – Output Pixel CLK all the time. Default 0x0
4	HSinVS	R/W	Block HSYNC at vertical blanking 1 – Output HSYNC all the time. Default 0x0
5	VHSbad	R/W	Block VSYNC and HSYNC for bad frame 1 – Output VSYNC/HSYNC for bad frame. Default 0x0
7-6	UpDown	R/W	Upside down or mirror the image enable 00 – normal (default) 01 – upside down 10 – mirror 11 – upside down and mirror

VSYNC Output Control Register – Address: a0H Default: 00H

Bit	Name	Read/Write	Description
4-0	VsP	R/W	VSYNC Position Range: 0 ~ 31 rows Default 0x0
7-5	VsW	R/W	VSYNC Width 000 – 1 row 001 – 2 rows 010 – 4 rows 011 – 8 rows >=100 – 16 rows Default is 0x0

Feature Description:

1. Window Control

Reg0x92	RowH[0]	Row Start High Byte
Reg0x93	RowL[7:0]	Row Start Low Byte
Reg0x94	ColH[1:0]	Column Start High Byte
Reg0x95	ColL[7:0]	Column Start Low Byte
Reg0x96	WinHH[0]	Window Height High Byte
Reg0x97	WinHL[7:0]	Window Height Low Byte
Reg0x98	WinWH[1:0]	Window Width High Byte
Reg0x99	WinWL[7:0]	Window Width Low Byte

These registers control the size and starting coordinates of the window. By changing these registers, you can get any image format smaller than or equal to VGA resolution.

2. Frame Control

By setting the bit0 of Reg0x91, the VSYNC output formats can be changed to be either cover the valid pixel data or not.

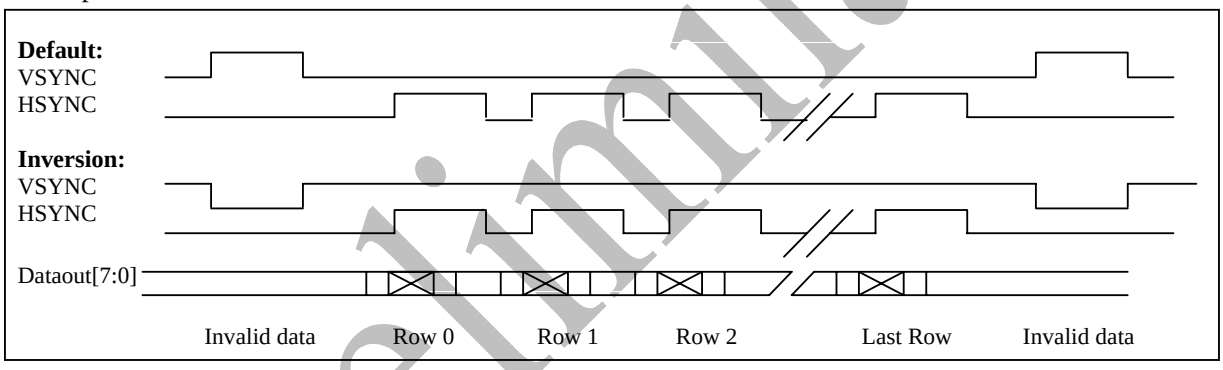


Figure 7. Different VSYNC formats

By setting the Reg0xa0, the VSYNC width and output position can be adjusted. The recommended way to adjust VSYNC output is to let VSYNC output at the Vertical Blanking period.

For example: When Reg0xa0 = 0x31,
Then, VsPos = 17*VsW from the default position (Reg0xa0 = 0x00),
and VsW' = 2*VsW.

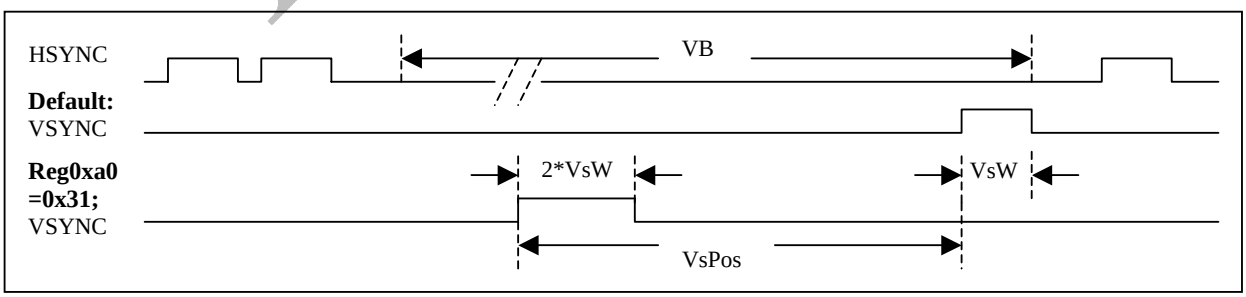


Figure 8. VSYNC output Control

3. Blanking Control

Reg0x81 control the blanking time in a row which is specified in terms of pixel clocks (Horizontal blanking).

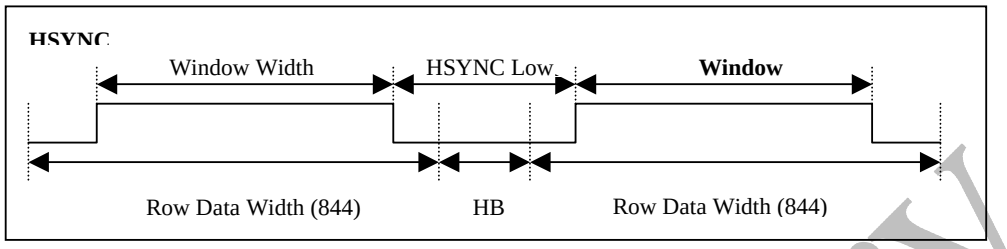


Figure 8. HSYNC Blanking Time (HB)

Reg0x82 control the blanking time between frames which is specified in terms of row readout time (Vertical blanking).

4. Mirror and Flips

The sensor module has 2 independent options for altering the readout order of the image data.
- Horizontally Mirrored readout. In this mode the columns in the pixel array are readout in reverse order.
- Vertically Flipped readout. In this mode the rows in the pixel array are readout in reverse order.

Thus the sensor module must support 4 possible pixel readout orders
1. Standard readout (Figure 12)
2. Horizontally Mirrored readout (Figure 13)
3. Vertically Flipped readout (Figure 14)
4. Horizontally Mirrored and Vertically Flipped readout (Figure 15)

Figure 10. Standard readout

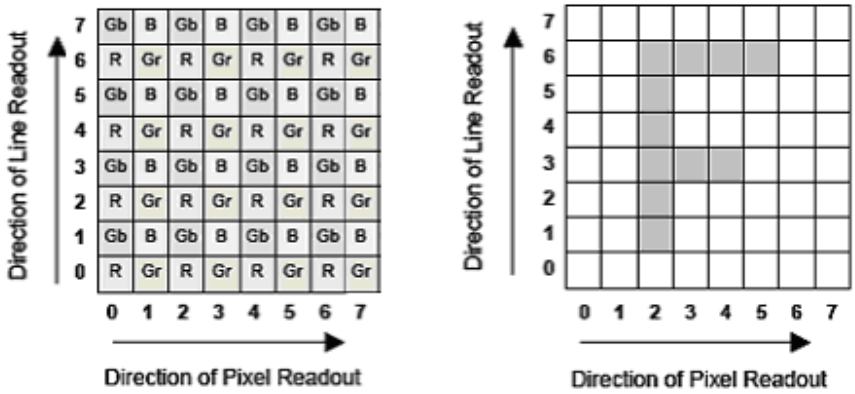


Figure 11. Horizontally Mirrored readout

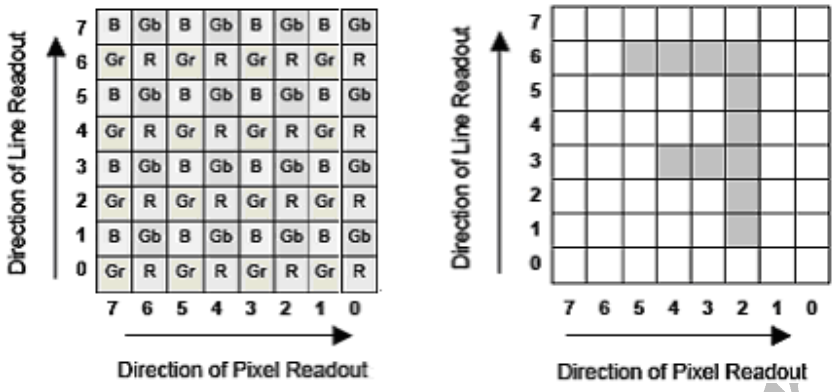


Figure 12. Vertically Flipped readout

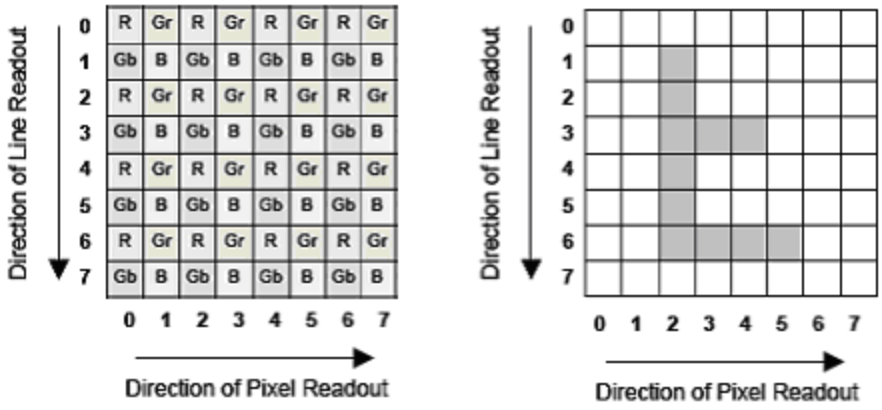


Figure 13. Horizontally Mirrored and Vertically Flipped readout

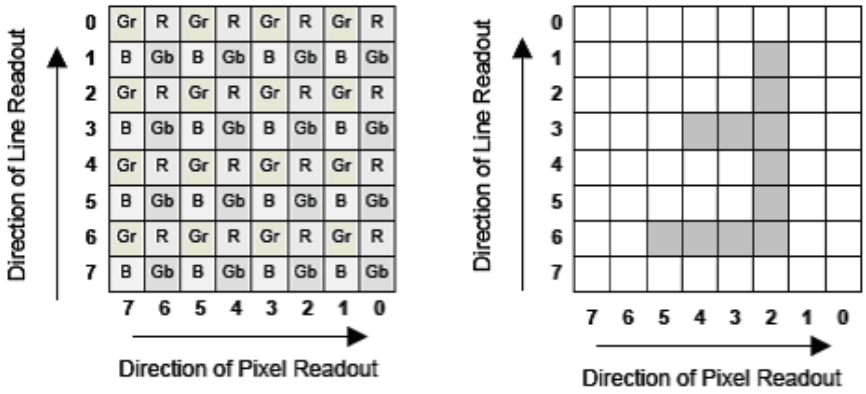


Figure 14. Pin-Out Diagram – 28-Pin PLCC

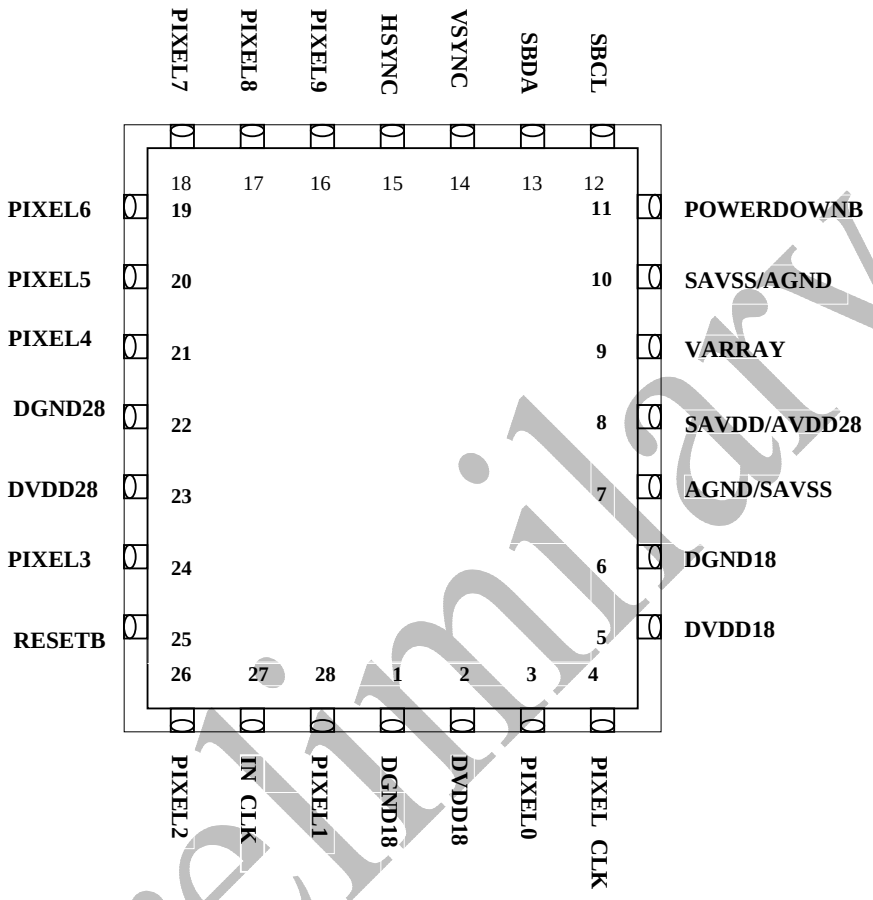


Table 6. Pin Description

NAME	TYPE	Description
DVDD28	Power	2.8V Digital I/O Pad power and ESD power supply.
DVDD18	Power	1.8V Digital Core and Pre-driver Power Supply.
AVDD28	Power	2.8V Analog circuit Power Supply.
SAVDD	Power	2.8V Analog ESD Power Supply.
SAVSS	Power	Analog ESD Ground.
VARRAY	Power	Pixel array Power Supply.
DGND28	Ground	2.8 V Digital I/O pad power and ESD Ground.
DGND18	Ground	1.8V Digital Core and Pre-driver Ground.
AGND	Ground	2.8V Analog circuit Ground.
IN_CLK	Input	External clock.
RESETB	Input	Chip level reset, Negative true.
POWERDOWNB	Input	Chip level Power down . Negative true.
SBCL	Input	Serial Bus clock in.
SBDA	Bi-direction	Serial Bus Data I/O.
ANN	Bi-direction	Minus terminal of the analog input / output. * Custom pad
ANP	Bi-direction	Positive terminal of the analog input/output. * Custom pad
PIXEL0	Output	Pixel Data Output Bit 0.
PIXEL1	Output	Pixel Data Output Bit 1.
PIXEL2	Output	Pixel Data Output Bit 2.
PIXEL3	Output	Pixel Data Output Bit 3.
PIXEL4	Output	Pixel Data Output Bit 4.
PIXEL5	Output	Pixel Data Output Bit 5.
PIXEL6	Output	Pixel Data Output Bit 6.
PIXEL7	Output	Pixel Data Output Bit 7.
PIXEL8	Output	Pixel Data Output Bit 8.
PIXEL9	Output	Pixel Data Output Bit 9.
VSYNC	Output	Active High during frame of valid pixel data.
HSYNC	Output	Active High during the line of selectable valid pixel data.
PIXEL_CLK	Output	The inverse output of the internal PIXEL_CLK.
STROBE	Output	Strobe signal

Figure 15. GC0303v1 Sensor Array Center

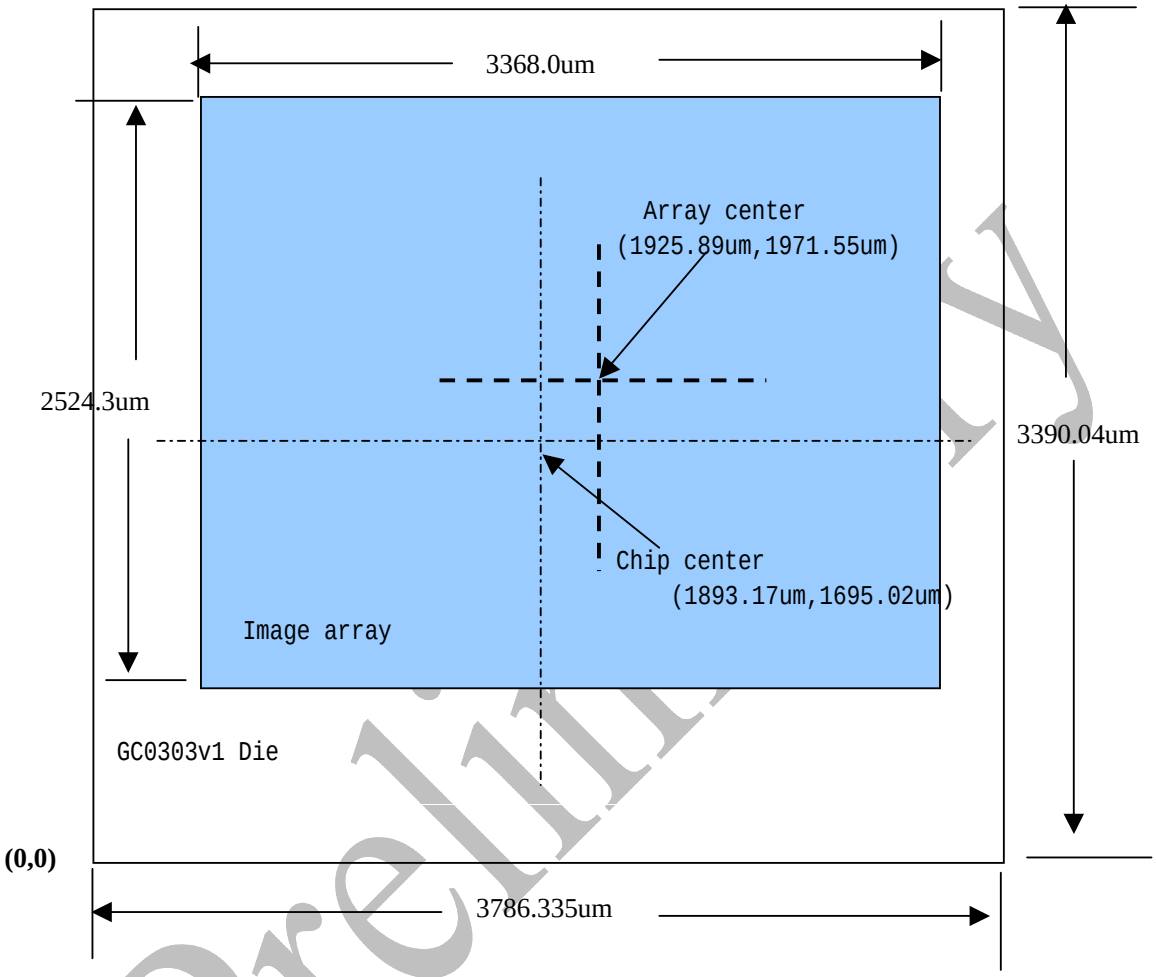


Figure 16. GC0303v1 PLCC Package